

CLAIMS:

1. A SiC semiconductor device comprising:
a semiconductor substrate having a P-type silicon carbide region, a gate insulation
5 layer formed on the silicon carbide region,
an effective P-type gate electrode formed on the gate insulation layer, an N-type
impurity region having an impurity concentration sufficient to form a buried channel region
in a semiconductor layer on a lower surface of the gate insulation layer, and
source and drain regions comprised of N-type impurity regions formed adjacent to the
10 gate insulation layer and gate electrode.

2. A device according to claim 1, wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not
more than 1.0, where the L_{bc} is a depth from an interface between the gate insulation layer and
the silicon carbide region to the buried channel region, and the X_j is a depth from the interface
between the gate insulation layer and the silicon carbide region to a junction of the source and
drain regions.

3. A device according to claim 2, wherein the gate electrode is comprised of
polycrystalline silicon in which boron or aluminum is diffused at a concentration within a
range of from $1 \times 10^{16} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$.

4. A device according to claim 2, wherein the gate electrode includes a silicide layer
of a refractory metal.

5. A device according to claim 4, wherein the refractory metal is tungsten,
molybdenum or titanium.

6. A device according to claim 2, wherein the gate electrode is formed of aluminum
or an alloy that contains aluminum.

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7. A device according to claim 2, wherein the buried channel region contains a diffusion of nitrogen, phosphorus or arsenic at a maximum concentration that is from $5 \times 10^{15} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$.

5 8. A device according to claim 2, wherein between the buried channel region and the source and drain regions there is a region having an impurity concentration that is not lower than a maximum impurity concentration of the impurity region used to form the buried channel region and not higher than an impurity concentration of the source or drain regions.

10 9. A device according to claim 7, wherein between the buried channel region and the source and drain regions there is a region having an impurity concentration that is not lower than a maximum impurity concentration of the impurity region used to form the buried channel region and not higher than an impurity concentration of the source or drain regions.

15 10. A device according to claim 8, wherein between the buried channel region and the source and drain regions there is a diffusion layer of nitrogen, phosphorus or arsenic at a maximum concentration that is from $5 \times 10^{16} \text{ cm}^{-3}$ to $1 \times 10^{19} \text{ cm}^{-3}$.

20 11. A device according to claim 9, wherein between the buried channel region and the source and drain regions there is a diffusion layer of nitrogen, phosphorus or arsenic at a maximum concentration that is from $5 \times 10^{16} \text{ cm}^{-3}$ to $1 \times 10^{19} \text{ cm}^{-3}$.

25 12. A device according to claim 7, wherein there is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel region.

30 13. A device according to claim 10, wherein there is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel region.

14. A device according to claim 11, wherein there is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel formation region.

15. A device according to claim 13, wherein there is a high-concentration P-type impurity diffusion region located adjacently under the buried channel region that includes an aluminum or boron diffusion layer having a maximum impurity concentration of $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{19} \text{ cm}^{-3}$.

16. A device according to claim 14, wherein there is a high-concentration P-type impurity diffusion region located adjacently under the buried channel region that includes an aluminum or boron diffusion layer having a maximum impurity concentration of $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{19} \text{ cm}^{-3}$.

17. A device according to claim 1, wherein the device is formed on a (11-20) surface or a (000-1) surface of a hexagonal or rhombohedral system or a (110) surface of a cubic system silicon carbide crystal.

18. A device according to claim 2, wherein the device is formed on a (11-20) surface or a (000-1) surface of a hexagonal or rhombohedral system or a (110) surface of a cubic system silicon carbide crystal.

19. A device according to claim 7, wherein the device is formed on a (11-20) surface or a (000-1) surface of a hexagonal or rhombohedral system or a (110) surface of a cubic system silicon carbide crystal.

20. A device according to claim 8, wherein the device is formed on a (11-20) surface or a (000-1) surface of a hexagonal or rhombohedral system or a (110) surface of a cubic system silicon carbide crystal.

21. A device according to claim 9, wherein the device is formed on a (11-20) surface or a (000-1) surface of a hexagonal or rhombohedral system or a (110) surface of a cubic system silicon carbide crystal.

5 22. A device according to claim 12, wherein the device is formed on a (11-20) surface or a (000-1) surface of a hexagonal or rhombohedral system or a (110) surface of a cubic system silicon carbide crystal.

10 23. A device according to claim 16, wherein the device is formed on a (11-20) surface or a (000-1) surface of a hexagonal or rhombohedral system or a (110) surface of a cubic system silicon carbide crystal.

24. A device according to claim 2, having a lateral resurf or lateral DMOS type MOSFET structure.

25. A device according to claim 6, having a lateral resurf or lateral DMOS type MOSFET structure.

20 26. A device according to claim 7, having a lateral resurf or lateral DMOS type MOSFET structure.

27. A device according to claim 8, having a lateral resurf or lateral DMOS type MOSFET structure.

25 28. A device according to claim 9, having a lateral resurf or lateral DMOS type MOSFET structure.

29. A device according to claim 12, having a lateral resurf or lateral DMOS type MOSFET structure.

30 30. A device according to claim 15, having a lateral resurf or lateral DMOS type MOSFET structure.

31. A device according to claim 16, having a lateral resurf or lateral DMOS type MOSFET structure.

32. A device according to claim 18, having a lateral resurf or lateral DMOS type MOSFET structure.

33. A device according to claim 8, having a DMOS type MOSFET structure.

34. A device according to claim 9, having a DMOS type MOSFET structure.

35. A device according to claim 12, having a DMOS type MOSFET structure.

36. A device according to claim 13, having a DMOS type MOSFET structure.

37. A device according to claim 14, having a DMOS type MOSFET structure.

38. A device according to claim 18, having a DMOS type MOSFET structure.

39. A device according to claim 8, wherein the gate electrode is formed of aluminum or an alloy that contains aluminum.

40. A device according to claim 9, wherein the gate electrode is formed of aluminum or an alloy that contains aluminum.

41. A device according to claim 12, wherein the gate electrode is formed of aluminum or an alloy that contains aluminum.

42. A device according to claim 15, wherein the gate electrode is formed of aluminum or an alloy that contains aluminum.